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**Complete If Known**

<b>Application Number</b>	<b>10/789,810</b>
<b>Filing Date</b>	<b>02/27/2004</b>
<b>First Named Inventor</b>	<b>Evgueni Goldberg</b>
<b>Art Unit</b>	<b>2129</b>
<b>Examiner Name</b>	<b>Omar F. Fernandez Rivas</b>
<b>Attorney Docket Number</b>	<b>CA7031042001</b>

[illegible][illegible]

5/2/2007

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STATEMENT BY APPLICANT**

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Filing Date	02/27/2004
First Named Inventor	Evgueni Goldberg
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Attorney Docket Number	CA7031042001

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
/OFR/	2	BAPTISTA, L. et al.; "The Interplay of Randomization and Learning of Real-World Instances of Satisfiability"; Proceedings of the AAAI Workshop on Leveraging Probability and Uncertainty in Computation; July 2000.	
/OFR/	3	BAYARDO, R. et al.; "Using CSP Look-Back Techniques to Solve Real-World SAT Instances"; Proceedings of the Fourteenth National Conference on Artificial Intelligence and Ninth Innovative Applications of Artificial Intelligence Conference; 1997; pp. 203-208; American Association for Artificial Intelligence Press; USA.	
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/OFR/	5	BIERE, A., et al.; "Symbolic Model Checking Using SAT Procedures Instead of BDDs"; Proceedings of Design Automation Conference - DAC'99; 1999; pp. 317 - 320; ACM; USA.	
/OFR/	6	BRAYTON, R.K., et al.; "Logic Minimization Algorithms for VLSI Synthesis"; Kluwer Academic Publishers, 1984; USA.	
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/OFR/	14	LI, C. M.; "A Constraint-Based Approach to Narrow Search Trees for Satisfiability"; Information Processing Letters 71; 1999; pp. 75 - 80; Volume 71; Elsevier Science B.V.; France.	
Examiner Signature	/Omar Fernandez Rivas/		Date Considered 5/2/2007

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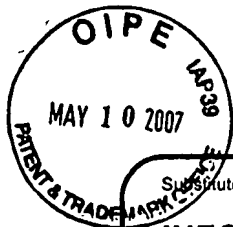
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/OFR/	15	MARQUES-SILVA, J.; "The Impact of Branching Heuristics in Propositional Satisfiability Algorithms"; Proceedings of the 9th Portuguese Conference on Artificial Intelligence (EPIA); September 1999; LNAI; pp. 62 - 74; 1695; Portugal.	
/OFR/	16	MARQUES-SILVA, J. P. et al.; "GRASP: A New Search Algorithm for Satisfiability"; CSE-TR-292-96; April 10, 1996; pp. 1 - 17; The University of Michigan; USA.	
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/OFR/	18	MOSKEWICZ, M. W. et al.; "Chaff: Engineering an Efficient SAT Solver"; Proceedings of the 38th Design Automation Conference - DAC '01; 2001; pp. 530 - 535; ACM; USA.	
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/OFR/	22	ZHANG, H.; "SATO: An Efficient Propositional Prover"; Proceedings of the 14th International Conference on Automated Deduction - CADE- 14; July 1997; pp. 272 - 275; Springer; Australia.	
/OFR/	23	SATLIB - Benchmark Problems; 2004; <a href="http://www.satlib.org/benchm.html">http://www.satlib.org/benchm.html</a> .	
/OFR/	24	The SAT-Ex site; 2004; <a href="http://www.lri.fr/~simon/satex/satex.php3">http://www.lri.fr/~simon/satex/satex.php3</a> .	
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Filing Date	02/27/2004
First Named Inventor	Evgueni GOLDBERG
Art Unit	2129
Examiner Name	Fernandez Rivas, Omar F.
Attorney Docket Number	CA7031042001

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/OFR/ ↓	1	GOLDBERG, E. "Testing Satisfiability of CNF Formulas by Computing a Stable Set of Points" Proceedings of the Conference Autated Deduction (CADE 2002) Copenhagen, DK, July 27-30, 2002, Vol. 2392, pp. 161-180	
	2	GOLDBERG, E. "Testing Satisfiability of CNF Formulas by Computing a Stable Set of Points" Annals of Mathematics and Artificial Intelligence, January 2005, Vol. 43, Issue 1-4, pp. 65-89	
	3	GOLDBERG, E. et al. "BerkMin: A Fast and Robust SAT-Solver" Proceedings of the design, Automation and Test In Europe Conference and Exhibition (DATE-2002) Paris, FR, March 4-8, 2002, pp. 142-149	
	4	GOLDBERG, E. "On Bridging Simulation and Formal Verification" Technical Report, University of California at Berkeley, February, 2007, CDNL-TR-2007-0212	
	5	Miroslav Velev's SAT Benchmarks, 3 pgs., located at: <a href="http://www.ece.cmu.edu/~mvelev/sat_benchmarks.html">http://www.ece.cmu.edu/~mvelev/sat_benchmarks.html</a>	
	6	GOLDBERG, E. "Determinization of Resolution by an Algorithm Operating on Complete Assignments" SAT-2006, pp. 90-05	
	7	ABRAMOVICI, M. et al. "Digital Testing and Testable Design, Wiley-IEEE Press, September, 1990, Title page, Table of Contents and Chapters 2 through 10 (pp. 9-455).	
	8	SELMAN, B. et al. "A New Method for Solving Hard Satisfiability Problems" The 10th National Conference on Artificial Intelligence (AAAI-92), San Jose, CA, July 12-16, 1992, pp. 440-446	
	9	SELMAN, B. et al. "Noise Strategies for Improving Local Search" The 12th National Conference on Artificial Intelligence (AAAI-94), Seattle, WA, July 31-August 4, 1994, pp. 337-343	
	10	SELMAN, B. et al. "Generating Hard Satisfiability Problems" Artificial Intelligence, 1996, Vol. 81, pp. 17-29	
/OFR/	11	SETOVICH, E.M. et al. "SIS: A System for Sequential Circuit Synthesis" Technical Report, University of California at Berkeley, 1992. Memorandum No. UCB/ERL M92/41	

Examiner Signature	/Omar Fernandez Rivas/	Date Considered	10/31/2007
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